Electronic Version
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Claims

[c1] What is claimed is:

1. A non-volatile memory cell, comprising:
a substrate, the substrate comprising a first region and a second region;
a plurality of isolation structures positioned on the substrate, the isolation structures comprising a first isolation structure positioned in the first region and a second isolation structure surrounding the second region;
a control gate positioned on the first isolation structure in the first region;
a first insulating layer positioned on the control gate;
a second insulating layer positioned on the portion of the substrate in the second region; and
a floating gate positioned on the first insulating layer and the second insulating layer.

[c2] 2. The non-volatile memory cell of claim 1, wherein the portion of the floating gate positioned in the first region is stacked above the control gate.

[c3] 3. The non-volatile memory cell of claim 1, wherein the floating gate comprises an opening positioned above the first insulating layer, and the opening is used to form a

wire therein to connect to the control gate.

[c4] 4. The non-volatile memory cell of claim 1, wherein the substrate comprises a well of a first conductivity type positioned in the first region and the second region.

[c5] 5. The non-volatile memory cell of claim 1, wherein the substrate comprises at least a doping region of a second conductivity type positioned beneath the second insulating layer.

[c6] 6. The non-volatile memory cell of claim 1, wherein the isolation structures comprise field oxide layers or shallow trench isolation structures.

[c7] 7. The non-volatile memory cell of claim 1, wherein the first insulating layer comprises a composite layer composed of an oxide layer, a silicon nitride layer, and a silicon oxide layer.

[c8] 8. The non-volatile memory cell of claim 1, wherein the second insulating layer comprises a tunneling oxide layer.

[c9] 9. A method of manufacturing a non-volatile memory cell, the method comprising:
providing a substrate, the substrate comprising a first region and a second region;

forming a plurality of isolation structures on the substrate, the isolation structures comprising a first isolation structure positioned in the first region and a second isolation structure surrounding the second region;
forming a control gate on the first isolation structure in the first region;
forming a first insulating layer on the control gate;
forming a second insulating layer on the portion of the substrate in the second region; and
forming a floating gate on the first insulating layer and the second insulating layer.

[c10] 10. The method of claim 9, wherein the method of forming the floating gate comprises:
forming a doped polysilicon layer on the substrate; and removing a portion of the doped polysilicon layer, and remaining a portion of the doped polysilicon layer on the first insulating layer and the second insulating layer to be the floating gate.

[c11] 11. The method of claim 10, wherein an opening is formed above the first insulating layer after removing the portion of doped polysilicon layer, the opening being used to form a wire therein to connect to the control gate.

[c12] 12. The method of claim 10, wherein the method of

forming the floating gate further comprises remaining a portion of the doped polysilicon layer in a high-voltage region to form at least a gate of an HV MOS transistor.

[c13] 13. The method of claim 12, wherein before forming the floating gate, the method further comprises forming a gate oxide layer with a thickness ranging between 450 and 550 angstroms in the high-voltage region.

[c14] 14. The method of claim 12, wherein the method of forming the floating gate further comprises remaining a portion of the doped polysilicon layer in a low-voltage region to form at least a gate of an LV MOS transistor.

[c15] 15. The method of claim 14, wherein before forming the floating gate, the method further comprises forming a gate oxide layer with a thickness ranging between 60 and 70 angstroms in the low-voltage region.

[c16] 16. The method of claim 14, wherein after forming the floating gate, the gate of the HV MOS transistor, and the gate of the LV MOS transistor, the method further comprises the following steps:
forming a plurality of double diffused drains in the high-voltage region;
forming a spacer on either side of the gate of the HV MOS transistor, the gate of the LV MOS transistor, and

the portion of the floating gate on the second insulating layer;

forming a plurality of doping regions in the high-voltage region, the low-voltage region, and the second region;

forming an inter-layer-dielectric layer on the entire substrate;

forming a plurality of contact holes in the inter-layer-dielectric layer to connect to the doping regions, the gate of the HV MOS transistor, the gate of the LV MOS transistor, and the control gate, respectively; and

forming a plurality of wires in the contact holes.

[c17] 17. The method of claim 9, wherein the isolation structures comprise field oxide layers or shallow trench isolation structures.

[c18] 18. The method of claim 9, wherein the first insulating layer comprises a composite layer composed of an oxide layer, a silicon nitride layer, and a silicon oxide layer.

[c19] 19. The method of claim 9, wherein the second insulating layer comprises a tunneling oxide layer.

[c20] 20. The method of claim 9, wherein the portion of the floating gate positioned in the first region is stacked above the control gate.